TED (21) -6041B
(Revision- 2021)

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DIPLOMA EXAMINATION IN ENGINEERING/TECHNOLOGY/MANAGEMENT/ COMMERCIAL PRACTICE – APRIL - 2024

VERILOG HDL & PROGRAMMABLE LOGIC DEVICES

[Maximum Marks : 75] [Time : 3 hours]

PART–A

I. Answer **all** the following questions in one word or sentence. Each question carries 1 mark.

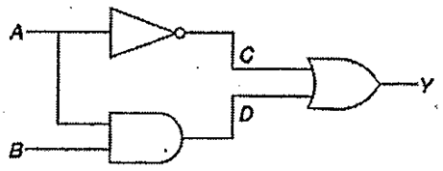
(9x1=9 marks)

		Module Outcome	Cognitive level
1	Define identifiers in Verilog.	M1.01	R
2	Mention any two lexical conventions.	M1.03	R
3	……is a low-level abstraction that describes design in terms of gates.	M2.03	R
4	`include “my_file.v” and `define WIDTH 8 are examples for……	M1.03	R
5	The continuous assignment that is used to drive net data type variables is the ……..statement.	M2.05	R
6	……..is the highest level of abstraction in Verilog modeling.	M3.01	R
7	Write one difference between initial and always block in Verilog.	M3.01	U
8	List any two applications of PAL.	M4.01	R
9	FPGA provides……..(**more**/**less**) logic resources and storage elements than CPLD.	M4.05	U

PART B

II. Answer **any Eight** questions from the following. Each question carries 3 marks.

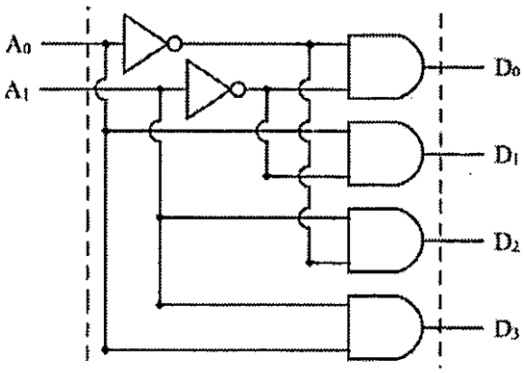
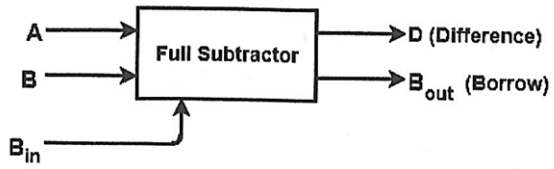
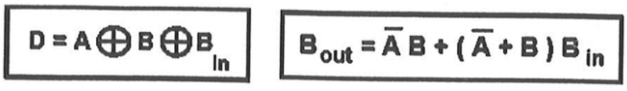
(8x3=24 marks)

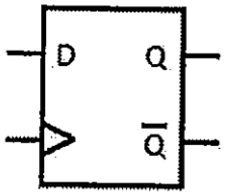
		Module Outcome	Cognitive level
1	Define System tasks with an example.	M1.02	R
2	Define Compiler directives.	M1.03	R
3	Design the logic circuit given below using Gate level modeling 	M2.03	A
4	Explain the architecture of a basic Verilog HDL Testbench with a block diagram.	M1.03	U
5	Write the syntax of **for loop** statement in Verilog with an example.	M3.04	R
6	List any 3 applications of FPGA.	M4.03	R
7	Draw CPLD architecture and mention the components.	M4.02	U
8	Differentiate between FPGA and CPLD.	M4.05	U
9	Compare PLA with PAL.	M4.01	U
10	List the components of Verilog module.	M1.04	R

PART C

Answer **all** questions from the following. Each question carries 7 marks.

(6x7=42marks)

		Module Outcome	Cognitive level
III	Explain the Design Flow of HDL.	M1.01	U
	OR		
IV	Explain the two Design methodologies of HDL.	M1.02	U
V	Design gate level modeling of the following circuit given below: 	M2.03	A
	OR		
VI	Write Verilog HDL description for full adder using Data flow modeling.	M2.08	A
VII	Explain the three ways of specifying delays in continuous assignment statements with examples.	M2.06	U
	OR		
VIII	Write Data flow modeling of 4:1 MUX in Verilog.	M2.08	A
IX	Explain about procedural assignments in behavioral modelling.	M3.02	U
	OR		
X	Design full subtractor using behavioral modeling with the following inputs and outputs.  	M3.05	A

XI	Explain Event timing control in Verilog.	M3.01	U
	OR		
XII	Write the Verilog HDL description of D flip flop in behavioral modelling. Symbol  Table of truth: clk | D | Q | $\overline{Q}$ 0 | 0 | Q | $\overline{Q}$ 0 | 1 | Q | $\overline{Q}$ 1 | 0 | 0 | 1 1 | 1 | 1 | 0	M3.04	A
XIII	Explain PAL architecture with diagram.	M4.01	U
	OR		
XIV	Explain FPGA architecture with the help of a diagram.	M4.03	U

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