TED (15/19) – 3042
(Revision – 2015/19)

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Reg.No……..
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DIPLOMA EXAMINATION IN ENGINEERING/TECHNOLOGY/MANAGEMENT/ COMMERCIAL PRACTICE, NOVEMBER – 2023

DIGITAL ELECTRONICS

[Maximum Marks : 100] [Time : 3 hours]

PART – A
(Maximum Marks : 10)

Marks

I. Answer **all** questions in one or two sentences. Each question carries 2 marks.

1. Draw the truth table and the symbol of an EX-OR gate.
2. What is meant by alphanumeric code? Give example.
3. Define fan-in and fan-out.
4. Draw the general representation of a sequential circuit.
5. Mention a limitation of binary weighted resistor type DAC. (5x2=10)

PART – B
(Maximum Marks : 30)

II. Answer any **five** of the following questions. Each question carries 6 marks.

1. State and explain De-Morgan's theorems.
2. Describe ECL logic family.
3. Explain a 3 bit encoder. Give an example.
4. Explain a D flip-flop with its diagram and characteristic table.
5. What is a shift register? Differentiate between left shift and right shift registers.
6. Differentiate between asynchronous and synchronous counters.
7. Define three specifications of a DAC.

(5x6=30)

PART – C

(Maximum Marks : 60)

(Answer **one full** question from each unit. Each full question carries 15 marks)

UNIT – I

III. (a) Realize basic gates using universal gates. (7)

(b) Perform the following conversions in number systems. (8)

(i) $(23A)_{16} = (\ )_2$ (ii) $(1110011101)_2 = (\ )_{16}$

(iii) $(785)_{10} = (\ )_2$ (iv) $(10001110)_2 = (\ )_{10}$

OR

IV. (a) Perform the following arithmetic operations by converting the given decimal numbers to binary. (8)

(i) 1's complement method subtraction of $(58)_{10} - (29)_{10}$

(ii) 2's complement method subtraction of $(78)_{10} - (45)_{10}$

(b) Reduce the given Boolean expression to its simplest form using k-map. (7)

$F = \Sigma\, m\,(3, 4, 10, 11, 13, 15) + \Sigma\, d\,(1, 2, 9, 12)$

UNIT – II

V. (a) Draw and explain a full adder circuit. Write its output equations and truth table. (8)

(b) Explain the working of CMOS NAND logic gate. (7)

OR

VI. (a) With logic diagram and truth table explain a 4 x 1 multiplexer. (9)

(b) Explain scales of integration and its classification. (6)

UNIT –III

VII. (a) Explain with block diagram the working of master slave JK flip flop. (9)

(b) Draw the logic diagram of a serial-in serial-out shift register. Write its truth table. (6)

OR

VIII. (a) Explain with logic diagram the working of a 4 bit Johnson counter. (9)

(b) Draw an SR latch using NOR gate and explain with truth table. (6)

UNIT – IV

IX. (a) Draw a mod-10 asynchronous counter using JK flip flop. Write its truth table. (6)

(b) Explain with diagram R-2R ladder type DAC. (9)

OR

X. (a) Draw a 3 bit synchronous counter using JK flip flop. Write its truth table. (6)

(b) Explain with diagram counter type ADC. (9)

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