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Reg.No.....
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DIPLOMA EXAMINATION IN ENGINEERING/TECHNOLOGY/MANAGEMENT/ COMMERCIAL PRACTICE, NOVEMBER - 2023

COMPUTER ARCHITECTURE

[Maximum marks: 100] [Time: 3 Hours]

PART – A
Maximum marks: 10

I (Answer ***all*** the questions in one or two sentences. Each question carries **2** marks)

1. List the elements of BUS Design.
2. What is RAID?
3. Define Seek Time.
4. Define Program Status Word.
5. List Flynn's classification of computer system. (5 x 2 = 10)

PART – B
Maximum marks: 30

II (Answer any ***five*** of the following questions. Each question carries **6** marks)

1. Draw and explain Von-Neumann Machine.
2. Compare DRAM and SRAM.
3. Explain the read and write operation in magnetic disk.
4. What is Compact Disk? Explain its working.
5. Draw the space time diagram and hardware organisation of four step instruction pipeline.
6. Explain the control and Status Registers inside CPU.
7. Explain micro operations. (5 x 6= 30)

PART – C
Maximum marks: 60

(Answer ***one full*** question from each unit**.** Each full question carries **15** marks)

UNIT –I

III. (a) Explain memory hierarchy. (6)

(b) Explain the elements of cache design. (9)

OR

IV. (a) Draw and explain the working of SRAM and DRAM memory cell. (8)

(b) Draw the structure of single cache organization and three level cache organization. (7)

UNIT-II

V. (a) Explain data organization and formatting mechanism in magnetic disk. (10)

(b) Define rotational delay, access time and transfer time. (5)

OR

VI. (a) Explain DMA controlled Data transfer. (6)

(b) Explain RAID levels 5, 6 and 10. (9)

UNIT-III

VII. (a) Explain about instruction cycle state diagram. (8)

(b) Explain user visible registers. (7)

OR

VIII. (a) Explain indirect cycle. (7)

(b) Explain instruction pipelining. (8)

UNIT-IV

IX. (a) Explain hardwired control unit implementation. (7)

(b) Draw and explain the general model of a control unit. (8)

OR

X. (a) Explain micro programmed control unit implementation. (8)

(b) Explain different types of multiple processor organisations. (7)
