TED (15/19) 3133
(Revision-2015/19)

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DIPLOMA EXAMINATION IN ENGINEERING/TECHNOLOGY/MANAGEMENT/ COMMERCIAL PRACTICE, NOVEMBER - 2023

DIGITAL COMPUTER PRINCIPLES

[Maximum marks: 100] [Time: 3 Hours]

PART – A
Maximum marks: 10

I (Answer ***all*** the questions in one or two sentences. Each question carries **2** marks)

1. Define the base of a number system.
2. Find the 2's complement of number $(100100)_{\mathbf{2}}$.
3. Define combinational logic circuit.
4. Define the modulus of a counter.
5. Name any error correcting codes used in data communication. (5 x 2 = 10)

PART – B
Maximum marks: 30

II (Answer any ***five*** of the following questions. Each question carries **6** marks)

1. Convert the decimal number $(41.6875)_{\mathbf{10}}$ to binary.
2. Explain a 4 bit serial in serial-out shift register.
3. Draw the circuit of a 4 bit adder/subtractor.
4. Simplify the Boolean function $F(A,B,C,D) = \sum m(1,2,6,7,8,13,14,15) + d(3,5,12)$.
5. Draw the circuit of a 3 bit asynchronous up counter using JK flip-flops.
6. Define the terms Resolution and accuracy of a DAC.
7. Write short notes on PLA. (5 x 6= 30)

PART – C
Maximum marks: 60

(Answer ***one full*** question from each unit**.** Each full question carries **15** marks)

UNIT –I

III. (a) Convert the following

(i) $(673.124)_{\mathbf{8}}$ to Binary
(ii) $(306.D)_{\mathbf{16}}$ to Octal
(iii) $(11001111.1001)_{\mathbf{2}}$ to Hexadecimal (9)

(b) Draw the logic symbol and truth table of two input NAND and NOR gate. (6)

OR

IV. (a) State and prove Demorgan's theorems. (9)

(b) Draw the logic symbol and truth tables of basic gates. (6)

UNIT-II

V. (a) Design a full subtractor with truth table and logic diagram. (9)

(b) Draw the circuit of a 2 to 4 line decoder and explain. (6)

OR

VI. (a) Draw the circuit of a Octal to Binary encoder and explain. (9)

(b) Express the Boolean function $F = A+\overline{B}\ C$ in a sum of min-terms. (6)

UNIT-III

VII. (a) Design a 3 bit down counter using JK flip flops. (8)

(b) Draw the circuit diagram of 4 bit ripple counter and explain. (7)

OR

VIII. (a) Explain the operation of master slave JK flip flop. (9)

(b) Compare synchronous and asynchronous counters. (6)

UNIT-IV

IX. (a) Explain the operation of counter type A/D convertor with neat sketch. (9)

(b) Explain the operation of R-2R ladder network. (6)

OR

X. (a) Explain the operation of successive Approximation type A/D converter. (9)

(b) Explain the operation of a static RAM cell. (6)
