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(Revision-2021)

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Reg.No.....

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DIPLOMA EXAMINATION IN ENGINEERING/TECHNOLOGY/MANAGEMENT/ COMMERCIAL PRACTICE, NOVEMBER - 2023

DIGITAL ELECTRONICS

[Maximum marks: 75] [Time: 3 Hours]

PART A

I. Answer all the following questions in one word or one sentence. Each question carries 1 mark

(9 x 1 = 9 Marks)

		Module outcome	Cognitive level
1	What value is to be considered for a "don't care condition''?..... (a) 0 (b) 1 (c) Either 0 or 1 (d) Any number except 0 an 1	M1.04	R
2	Signed negative binary number is recognised by its..... (a) MSB (b) LSB (c) Byte (d) Nibble	M1.02	R
3	The full form of ECL is	M2.02	R
4	How many select lines would be required for an 8-line-to-1-line multiplexer?	M2.04	U
5	In a J-K flip-flop, if J=K the resulting flip-flop is referred to as ……	M3.02	A
6	Which type of shift register the Q or Q^1 output of one stage is not connected to the input of the next stage.	M3.03	A
7	Which Flip-flop do not have No change condition?	M3.03	R
8	How many flip-flops are required to make a MOD-32 binary counter?	M4.03	U
9	In a DRAM, What is the state of R/W during a read operation?	M4.04	R

PART B

II. Answer any eight questions from the following. Each question carries 3 marks.

(8 x 3 = 24 Marks)

		Module outcome	Cognitive level
1	Convert 567.25_{10} to Hexa decimal number	M1.01	U
2	Convert to binary and subtract in 2's compliment method - 96_{10} - 47_{10}	M1.02	U
3	Construct OR gate and EX-OR gate using NAND gate	M1.03	R
4	Compare TTL and CMOS Logic familes	M2.01	R
5	Design a Half adder circuit.	M2.04	A
6	Draw the logic diagram of 4x1 multiplexer.	M2.04	R
7	Compare Combinational and sequential circuits.	M3.01	R

8	Explain the operation of SR flip flop using NOR gates Logic diagram and Truth Table.	M3.02	U
9	Compare synchronous and Asynchronous counters.	M4.01	R
10	What is Flash and cache memory?	M4.01	R

PART C

Answer all questions. Each question carries seven marks

(6 x 7 = 42 Marks)

		Module outcome	Cognitive level
III	Minimize the function using K map. $F = \sum m(1,2,3,4,7,11,13) + d(9,15)$	M1.01	A
	OR		
IV	Convert the following (i) $(10101.101)_2 = (\_\_\_)_{10}$ (ii) $(4321)_8 = (\_\_\_)_2$ (iii) $(A35)_{16} = (\_\_\_)_2$ (iv) $(89.625)_{10} = (\ )_2$	M1.04	U
V	Explain about BCD and Excess-3 codes with examples.	M1.02	U
	OR		
VI	Prove demorgan's theorems.	M1.04	U
VII	Explain the terms (i) Fan-in and Fan-out (ii) Propagation delay (iii) Power dissipation and (iv) Noise margin	M2.02	R
	OR		
VIII	Draw the logic diagram and explain 4 bit parallel binary adder.	M2.04	U
IX	Draw a full Subtractor Circuit and Explain.	M2.04	U
	OR		
X	Draw a 4 bit Serial in-Serial out (SISO) Shift register.	M3.04	U
XI	Explain the working of JK Flip Flop with diagram and Truth Table.	M3.02	U
	OR		
XII	What is a shift register? What are its various types? Explain.	M3.03	R
XIII	Design a 3 bit ripple up counter.	M4.02	A
	OR		
XIV	Design a Mod 10 Asynchronous counter using J K flip-flops.	M4.02	A

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