TED (21)3131
(Revision – 2021)

2110220197

Reg. No……
Signature …….

DIPLOMA EXAMINATION IN ENGINEERING/TECHNOLOGY/ MANAGEMENT/COMMERCIAL PRACTICE, NOVEMBER – 2023

COMPUTER ORGANISATION

[Maximum Marks: **75**] [Time: **3** Hours]

PART-A

I. Answer *all* the following questions in one word or one sentence. Each question carries *'one'* mark.

(9 x 1 = 9 Marks)

		Module Outcome	Cognitive level
1.	List the functional units of a computer system.	M1.01	R
2.	What is seek time?	M1.09	R
3.	Define raster scan.	M2.05	R
4.	USB stands for.....	M2.04	R
5.	List the stages of an Instruction Cycle.	M3.02	U
6.	List any two registers involved in fetch operation.	M3.02	R
7.	What is program counter?	M3.01	R
8.	The word length of 8086 microprocessor is.....Bits.	M4.01	U
9.	Which are the index registers of 8086.	M4.02	R

PART-B

II. Answer any *eight* questions from the following. Each question carries *'three'* marks.

(8 x 3 = 24 Marks)

		Module Outcome	Cognitive level
1.	Explain single bus interconnection structure.	M 1.03	R
2.	Compare DRAM and SRAM.	M 1.05	R
3.	Explain the concept of Program controlled I/O.	M2.01	U
4.	Draw the internal structure of a CPU.	M3.01	R
5.	What are the operations involved in the transfer of content of register R1 to register R2.	M3.01	U
6.	Give the steps involved in execution of an instruction.	M3.02	U
7.	Interpret the terms control word, micro routine and control store.	M3.03	R
8.	Mention the purpose of different segment registers of 8086.	M4.02	U
9.	Describe multicore processing concepts.	M4.04	U
10.	Outline any three features Pentium processor.	M4.03	R

PART-C

Answer all questions from the following. Each question carries *'seven'* marks.

(6 x 7 = 42 Marks)

		Module Outcome	Cognitive level
III.	Outline the memory hierarchy with respect to speed, size and cost with neat diagram.	M1.06	U
	OR		
IV.	Explain the principles of cache memory.	M1.07	U
V.	Define a cell in semiconductor memory and with a neat diagram explain organization of cells in a chip.	M1.05	R
	OR		
VI.	Explain how data is organised in a disk with the help of a diagram and accessed.	M1.09	R
VII.	Explain I/O interfacing with a neat sketch. What is memory-mapped I/O?	M2.01	U
	OR		
VIII.	Illustrate how interrupts from multiple devices are handled.	M2.02	U
IX.	What is Direct Memory Access? Explain cycle stealing and block/burst mode of operation.	M2.03	R
	OR		
X.	Explain the features of SCSI.	M2.04	R
XI.	Explain the functioning of hardwired control unit with diagram.	M3.03	U
	OR		
XII.	Explain the concept of instruction pipelining.	M3.04	U
XIII.	Mention the purposes of conditional flags of 8086.	M4.02	U
	OR		
XIV.	Draw the internal block diagram of 8086 microprocessor.	M4.02	U

****